WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

an impurity diffusion layer having first conductivity type, and being formed in the semiconductor substrate to have a predetermined depth;

a channel well layer having second conductivity type, and being formed in the semiconductor substrate to generate a PN junction at an interface with the impurity diffusion layer;

a source diffusion layer having first conductivity type, being formed in the channel well layer, and for defining a channel forming region in the channel well layer;

a drain-contact layer having first conductivity type, and being formed in the impurity diffusion layer;

an insulating isolation film formed on the impurity diffusion layer between the channel well layer and the drain-contact layer; and

a gate electrode formed on the channel forming region of the channel well layer with a gate oxide film interposed therebetween, and being protruded onto the insulating isolation film,

wherein the gate electrode is formed so that a maximum electric field point in the neighborhood of a surface of the semiconductor substrate occurs at substantially the center portion of a region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source diffusion layer and the drain-contact layer, and the source diffusion layer and the gate electrode are at substantially identical potential.

2. A semiconductor device comprising:

a semiconductor substrate;

an impurity diffusion layer having first conductivity type, and being formed in the semiconductor substrate to have a predetermined depth;

a channel well layer having second conductivity type and being formed in the semiconductor substrate to generate a PN junction at an interface with the impurity diffusion layer;

a source diffusion layer having first conductivity type, being formed in the channel well layer, and for defining a channel forming region in the channel well layer;

a drain-contact layer having first conductivity type, and being formed in the impurity diffusion layer;

an insulating isolation film formed on the impurity diffusion layer between the channel well layer and the drain-contact layer; and

a gate electrode formed on the channel forming region of the channel well layer with a gate oxide film interposed therebetween, and is protruded onto the insulating isolation film,

wherein the gate electrode is formed so that a peak of carrier generation rate in the neighborhood of a surface of the semiconductor substrate occurs at lower region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source diffusion layer and the drain-contact layer, and the source diffusion layer and the gate electrode are substantially at identical potential.

3. A semiconductor device comprising:

a semiconductor substrate;

an impurity diffusion layer having first conductivity type, and being formed in the semiconductor substrate to have a predetermined depth;

a channel well layer having second conductivity type and being formed in the semiconductor substrate to generate a PN junction at an interface with the impurity diffusion layer;

a source diffusion layer having first conductivity type, being formed in the channel well layer, and for defining a channel forming region in the channel well layer;

a drain-contact layer having first conductivity type, and being formed in the impurity diffusion layer;

an insulating isolation film formed on the impurity diffusion layer between the channel well layer and the drain-contact layer; and

a gate electrode formed on the channel forming region of the channel well layer with a gate oxide film interposed therebetween, and is protruded onto the insulating isolation film,

wherein the gate electrode is formed so that a carrier flow in the neighborhood of a surface of the semiconductor substrate contains a component toward an opposite side direction of the insulating isolation film, when a predetermined bias voltage is applied between the source diffusion layer and the drain-contact layer, and the source diffusion layer and the gate electrode are substantially at identical potential.

4. A semiconductor device according to claim 1, wherein the insulating isolation film is partially used as the gate oxide film.

5. A semiconductor device according to claim 1, wherein a junction depth of the impurity diffusion layer is set to shallow than that of the channel well layer.

6. A semiconductor device according to claim 1, wherein the impurity diffusion layer is formed in a well shape in the semiconductor substrate.

7. A semiconductor device according to claim 1, wherein:

the semiconductor substrate is an SOI substrate formed from a supporting substrate and a semiconductor layer with an insulating film interposed therebetween, and

the impurity diffusion layer is formed in the semiconductor layer.

8. A semiconductor device according to claim 7, wherein the supporting substrate is made of semiconductor material, and

the supporting substrate includes a potential fixing electrode formed on its back surface to fix a potential of the supporting substrate with a predetermined level.

9. A semiconductor device according to claim 1, further comprising:

another impurity diffusion layer having second conductivity type, and being formed in the semiconductor substrate;

another channel well layer having first conductivity type and being formed in the semiconductor substrate to generate a PN junction at an interface with the another impurity diffusion layer;

another source diffusion layer having second conductivity type, being formed in the another channel well layer, and for defining another channel forming region in the another channel well layer;

another drain-contact layer having second conductivity type, and being formed in the another impurity diffusion layer;

another insulating isolation film formed on the another impurity diffusion layer between the another channel well layer and the another drain-contact layer; and

another gate electrode formed on the another channel forming region of the another channel well layer with the gate oxide film interposed therebetween, and is protruded onto the another insulating isolation film.

10. A semiconductor device according to claim 1, wherein the gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

11. A semiconductor device according to claim 2, wherein the gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

12. A semiconductor device according to claim 3, wherein the gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

13. A semiconductor device according to claim 10, wherein the gate electrode is formed so that a protrusion amount onto the insulating isolation film is set to substantially a half of a width size of the insulating isolation film.

14. A semiconductor device according to claim 11, wherein the gate electrode is formed so that a protrusion amount onto the insulating isolation film is set to substantially a half of a width size of the insulating isolation film.

15. A semiconductor device according to claim 12, wherein the gate electrode is formed so that a protrusion amount onto the insulating isolation film is set to substantially a half of a width size of the insulating isolation film.

16. A method of manufacturing a semiconductor device, comprising steps of:

basic structure forming step for forming a basic structure of a semiconductor device on a semiconductor wafer;

passivation film forming step for forming a final passivation film that transmits ultra violet rays on an uppermost of the basic structure;

bias voltage applying step for applying to the semiconductor device with a bias voltage having a predetermined level voltage that can maintain the semiconductor device with turning off; and

ultra violet rays radiation step conducted after the bias voltage applying step, for radiating ultra violet rays to the basic structure of the semiconductor device through the final passivation film.

17. A method of manufacturing a semiconductor device, comprising steps of:

basic structure forming step for forming a basic structure of a semiconductor device on a semiconductor wafer;

passivation film forming step for forming a final passivation film that transmits ultra violet rays on an uppermost of the basic structure;

division step for dividing the semiconductor device into a plurality of semiconductor chips;

packaging step for mounting the semiconductor chip on a package having a transmitting portion that can transmit ultra violet rays at least on the final passivation film side;

bias voltage applying step for applying to the semiconductor device with a bias voltage having a predetermined level voltage that can maintain the semiconductor device with turning off; and

ultra violet rays radiation step conducted after the bias voltage applying step, for radiating ultra violet rays to the basic structure of the semiconductor device through the transmitting portion and the final passivation film.

18. A method of manufacturing a semiconductor according to claim 16, wherein:

the semiconductor is a switching element selected from one of a LDMOS FET (Lateral Double-Diffused Metal Oxide Semiconductor Field effect Transistor) and a VDMOS FET (Vertical Double-Diffused Metal Oxide Semiconductor Field effect Transistor), and

the bias voltage applying step applies between a source and a drain of the switching element with the bias voltage having a predetermined level voltage that can maintain the switching element with turning off.

19. A method of manufacturing a semiconductor according to claim 16, wherein the ultra violet rays radiation step radiates ultra violet rays having a band whose wave length of 253.7 nm.